JRC

MUSES72320

MUSES

±18V Operation 2-Channel Electronic Volume

■ GENERAL DESCRIPTION

The **MUSES72320** is a ±18V operation 2-channel electronic volume, which is optimized for high-end audio and professional audio applications with advanced circuitry and layout. The **MUSES72320** performs low noise and low distortion characteristics and with resistance ladder circuit.

All of functions are controlled via three-wired serial bus. Selectable 8-Chip address is available for using four chips on same serial bus line.

It's suitable for highly linear volume control of Hi-fi audio systems.

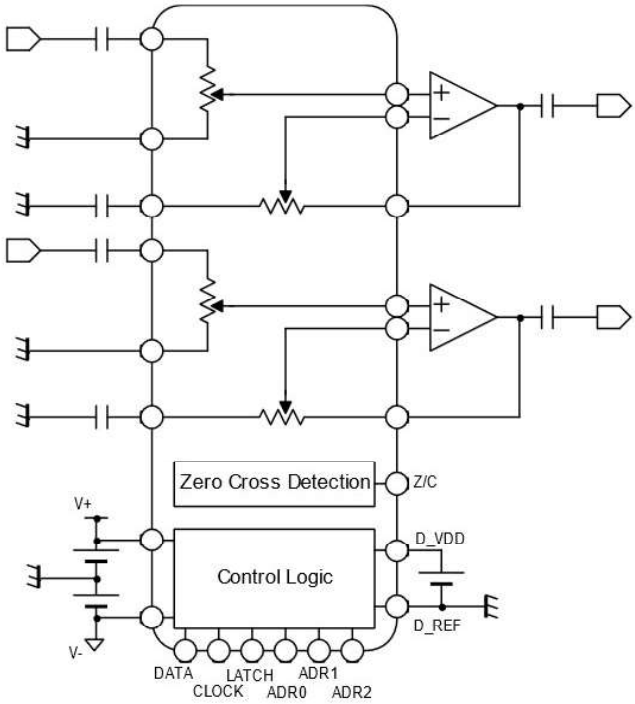
■ PACKAGE OUTLINE

MUSES72320V

■ FEATURES

● Operating Voltage	±8.5 to ±18V
● 3-Wired Serial Control	Chip Address Select Function
● Selectable 8-Chip Address	Available for using eight chips on same serial bus line
● Low Output Noise	*It conforms to the characteristic of an external operational amplifier.
● Low Distortion	*It conforms to the characteristic of an external operational amplifier.
● Volume	0dB to −111.5dB /0.25dBstep, MUTE +31.5 to 0dB / 0.5dBstep
● Channel Separation	-120dB typ.
● Zero Cross Detection circuit Detection	
● CMOS Technology	
● Package Outline	SSOP32

■ BLOCK DIAGRAM



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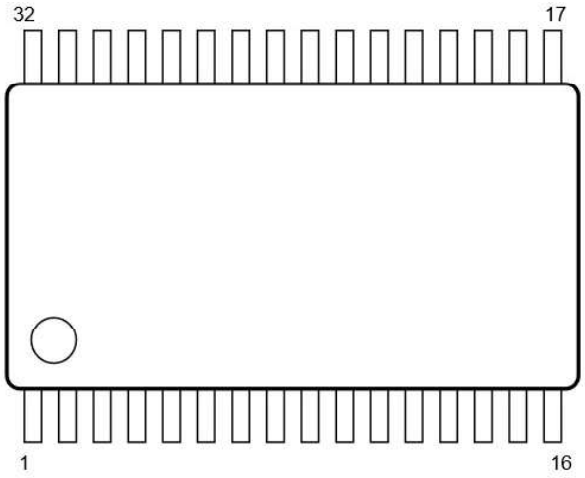
■ PIN FUNCTION



No.	SYMBOL	FUNCTION	No.	SYMBOL	FUNCTION
1	Z/C REFL	Lch Zero Cross Detection circuit Reference Voltage	17	D_VDD	Digital block Power Supply
2	L_REF	Lch Reference Voltage	18	DATA	Control data signal input
3	L+	Lch Opamp non-inverting input connect terminal	19	CLOCK	Clock signal input
4	L_REF	Lch Reference Voltage	20	LATCH	Latch signal input
5	L-	Lch Opamp inverting input connect terminal	21	D_REF	Digital block Reference Voltage
6	L_REF	Lch Reference Voltage	22	V+	Power Supply (+)
7	OutL	Lch output	23	InR	Rch input
8	DCCAP_L	Switching noise rejection capacitor (Lch)	24	V+	Power Supply (+)
9	DCCAP_R	Switching noise rejection capacitor (Rch)	25	V -	Power Supply (-)
10	OutR	Rch output	26	InL	Lch input
11	R_REF	Rch Reference Voltage	27	V -	Power Supply (-)
12	R-	Rch Opamp inverting input connect terminal	28	D_CAP	Digital block Noise Rejection Capacitor terminal
13	R_REF	Rch Reference Voltage	29	ADR2	Chip address setting terminal 2
14	R+	Rch Opamp non-inverting input connect terminal	30	ADR1	Chip address setting terminal 1
15	R_REF	Rch Reference Voltage	31	ADR0	Chip address setting terminal 0
16	Z/C REFR	Rch Zero Cross Detection circuit Reference Voltage	32	Z/C	Zero Cross Detection circuit ON/OFF setting terminal

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_+/V_-	+20/-20	V
Maximum Input Voltage	V_{IM}	V_+/V_-	V
Power Dissipation	P_D	1000 NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting	mW
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
◆ Power Supply (Ta=25°C, V^+/V^-=±15V, unless otherwise specified)						
Operating Voltage	V_+/V_-		±8.5	±15.0	±18.0	V
Supply Current 1	I_{CC}	No signal	-	2.0	10.0	mA
Supply Current 2	I_{EE}	No signal	-	2.0	10.0	mA
◆ Input/Output Characteristics 1 (Ta=25°C,V^+/V^-=±15V, V_{IN}=2Vrms, f=1kHz, Volume=0dB, Gain=0dB, V_{OUT} with MUSES01, R_L=47kΩ, unless otherwise specified)						
Maximum Input Voltage	V_{IM}	f=1kHz,THD=1% Volume=-20dB	10.9	-	-	Vrms
Voltage Gain 1	G_{V1}	V_{IN}=2Vrms, f=1kHz	-0.5	0	+0.5	dB
Voltage Gain 2	G_{V2}	V_{IN}=200mVrms, f=1kHz Gain=+15dB	+14	+15	+16	dB
Voltage Gain Error 1	ΔG_{V1}	V_{IN}=2Vrms, f=1kHz	-0.5	0	+0.5	dB
Voltage Gain Error 2	ΔG_{V2}	V_{IN}=2Vrms, f=1kHz Volume=-60dB	-1.0	0	+1.0	dB
Maximum Attenuation	A_{TT}	V_{IN}=4Vrms, f=1kHz Volume=-111.5dB, A-weight	-	-111.5	-	dB
Mute level	Mute	f=1kHz, V_{IN}=4Vrms Volume=Mute, A-weight	-	-120	-	dB
Channel Separation 1	CS1	f=1kHz, V_{IN} =2Vrms, Rg=0Ω A-weight	-	-110	-90	dB
Channel Separation 2	CS2	f=20kHz, V_{IN} =2Vrms, Rg=0Ω	-	-90	-	dB
Input Impedance	R_{IN}	23pin, 26pin	14	20	-	kΩ
◆ Input/Output Characteristics 2 (Ta=25°C,V^+/V^-=±15V, V_{IN}=2Vrms, f=1kHz, Volume=0dB, Gain=0dB, V_{OUT} with MUSES01, R_L=47kΩ, unless otherwise specified)						
Maximum Output Voltage	V_{OM}	f=1kHz,THD=1% Volume=-6dB, Gain=+6dB	-	9.5	-	Vrms
Total Harmonic Distortion 1	THD1	f=1kHz,V_{IN}=1Vrms BW=400Hz-30kHz	-	0.0005	-	%
Total Harmonic Distortion 2	THD2	f=10kHz,V_{IN}=1Vrms BW=400Hz-30kHz	-	0.001	-	%

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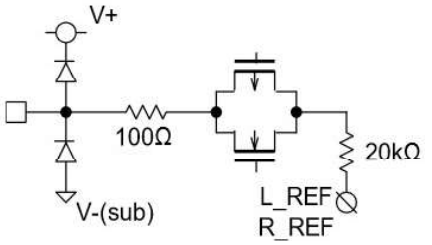
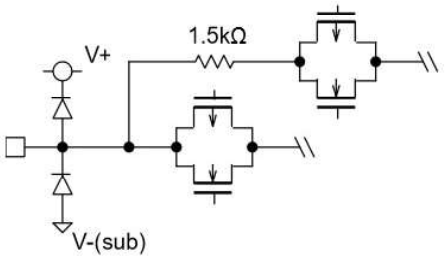
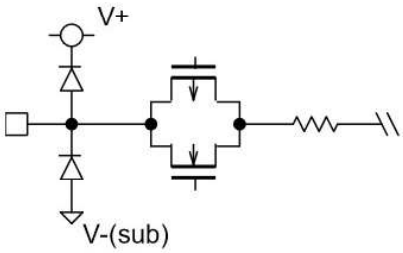
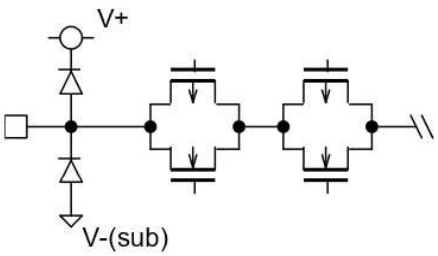
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
◆ Input/Output Characteristics 3 (Ta=25°C, V^+/V^-=±15V, V_{IN}=2Vrms, f=1kHz, Volume=0dB, V_{OUT} : 3pin, 14pin, R_L=100kΩ, unless otherwise specified)						
Output Noise1	V_{NO1}	Rg=0Ω, A-weight	-	-118 (1.26μ)	-100 (10μ)	dBV (Vrms)
Output Noise2	V_{NO2}	Volume=-111.5dB Rg=0Ω, A-weight	-	-118 (1.26μ)	-	dBV (Vrms)

■ Logic Control Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
◆ Digital block Power Supply Characteristics						
D_VDD Terminal Input Voltage	V_{DVDD}	17pin Terminal Input	-	-	0.8*V+	V
D_REF Terminal Input Voltage	V_{DREF}	21pin Terminal Input	V -	-	-	V
Digital block Supply Voltage Range	V_{DD}	$V_{DD} = V_{DVDD} - V_{DREF}$	3.0	5.0	6.0	V
◆ Logic Control Terminal Characteristics (Ta=25°C, V^+/V^-=±15V, V_{DREF} =0V, unless otherwise specified)						
High Level Input Voltage1	V_{IH1}	DATA, CLOCK, LATCH	0.7*V_{DD}	-	V_{DD}	V
Low Level Input Voltage1	V_{IL1}	DATA, CLOCK, LATCH	0	-	0.3*V_{DD}	V
◆ Chip Address / Zero cross Terminal Characteristics (Ta=25°C, V^+/V^-=±15V, V_{DREF} =0V, unless otherwise specified)						
High Level Input Voltage2	V_{IH2}	ADR0, ADR1, ADR2, Z/C	0.7*V_{DD}	-	V^+	V
Low Level Input Voltage2	V_{IL2}	ADR0, ADR1, ADR2, Z/C	0	-	0.3*V_{DD}	V

■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
23 26	InR InL	Rch input Lch input		0V
2 4 6 11 13 15	L_REF R_REF	Lch Reference Voltage Rch Reference Voltage		0V
3 14	L+ R+	Lch Opamp non-inverting input connect terminal Rch Opamp non-inverting input connect terminal		0V
5 12	L- R-	Lch Opamp inverting input connect terminal Rch Opamp inverting input connect terminal		0V

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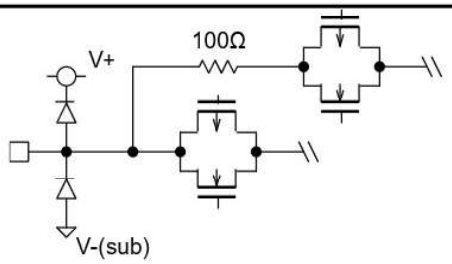
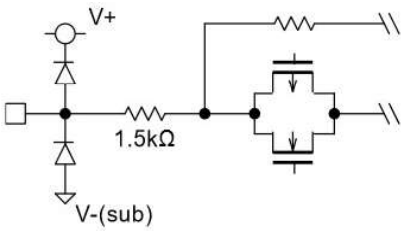
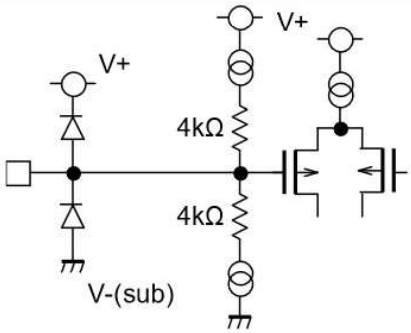
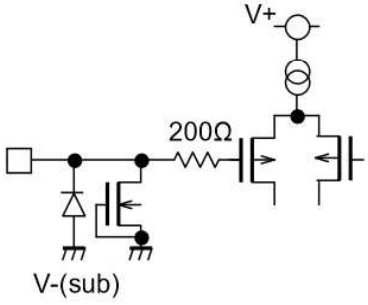
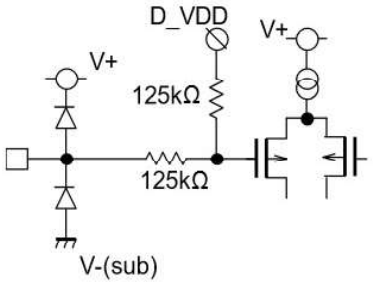
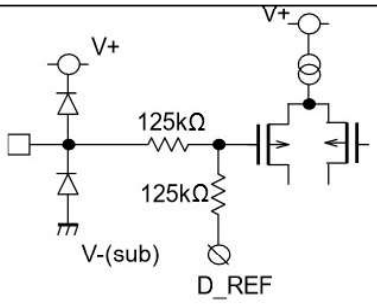
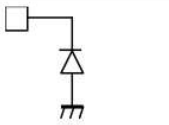
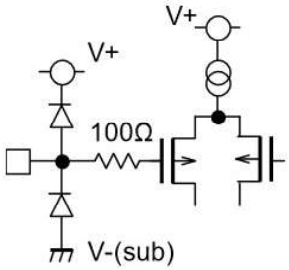
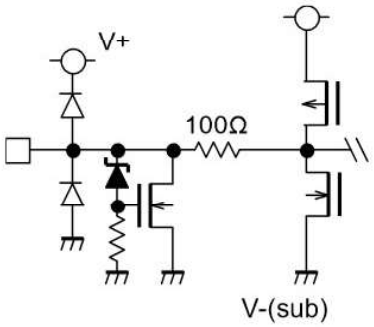
■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
7 10	OutL OutR	Lch output Rch output		0V
8 9	DCCAP_L DCCAP_R	Switching noise rejection capacitor (Lch) Switching noise rejection capacitor (Rch)		0V
16 1	Z/C REFR Z/C REFL	Rch Zero Cross Detection circuit Reference Voltage Lch Zero Cross Detection circuit Reference Voltage		0V
18 19 20	DATA CLOCK LATCH	Control data signal input Clock signal input Latch signal input		-

■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
21	D_REF	Digital block Reference Voltage		-
17	D_VDD	Digital block Power Supply		-
22 24	V^+	Power Supply (+)		V^+
32 29 30 31	Z/C ADR2 ADR1 ADR0	Zero Cross Detection circuit ON/OFF setting terminal Chip address setting terminal 2 Chip address setting terminal 1 Chip address setting terminal 0		-
28	D_CAP	Digital block Noise Rejection Capacitor terminal		0V

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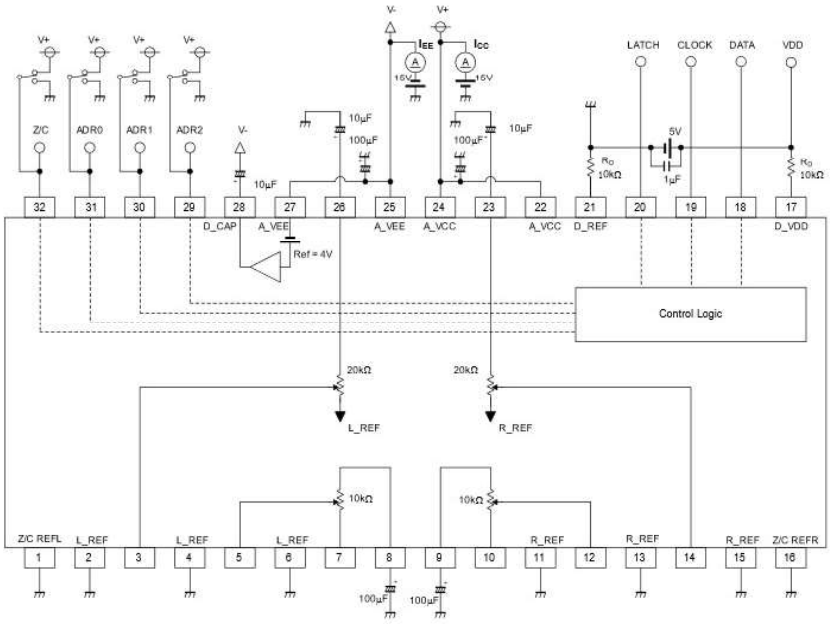
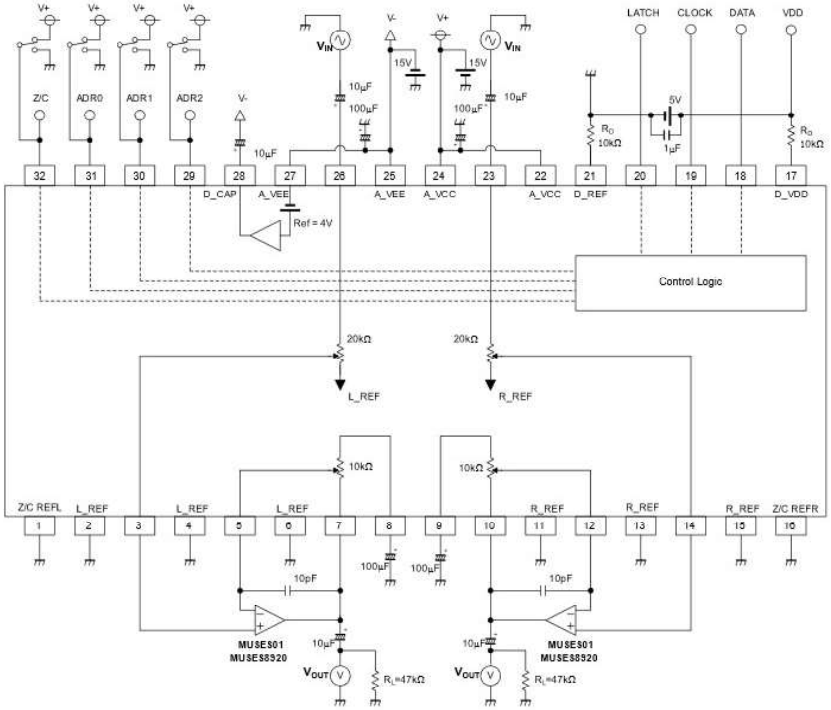
■ TEST CIRCUIT 1

Supply Current 1 (I_{CC}) , Supply Current 1 (I_{EE})



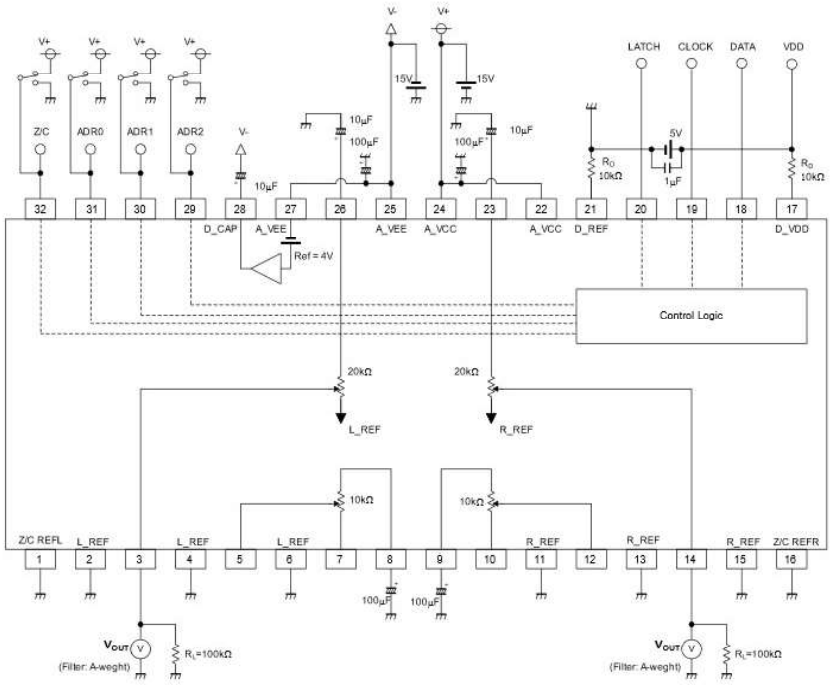
■ TEST CIRCUIT 2

Maximum Input Voltage (V_{IM}), Maximum Output Voltage (V_{OM}), Voltage Gain 1 (G_{V1}), Voltage Gain 2 (G_{V2}), Maximum Attenuation (A_{TT}), Mute level Mute), Total Harmonic Distortion 1(THD1), Total Harmonic Distortion 2(THD2)



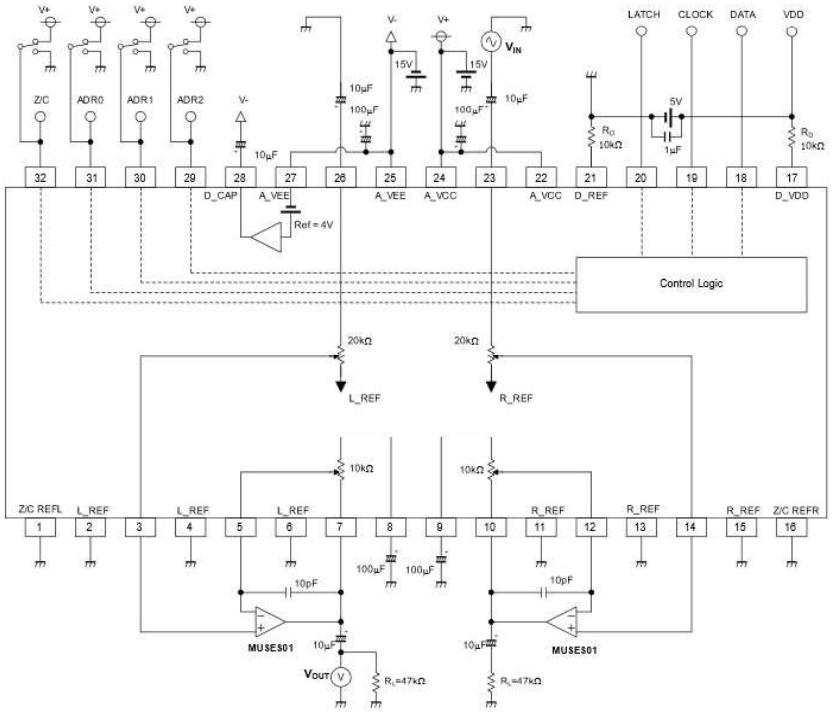
■ TEST CIRCUIT 3

Output Noise 1(V_{NO1}), Output Noise 1(V_{NO2})



■ TEST CIRCUIT 4

Channel Separation 1(CS1), Channel Separation 2(CS2)



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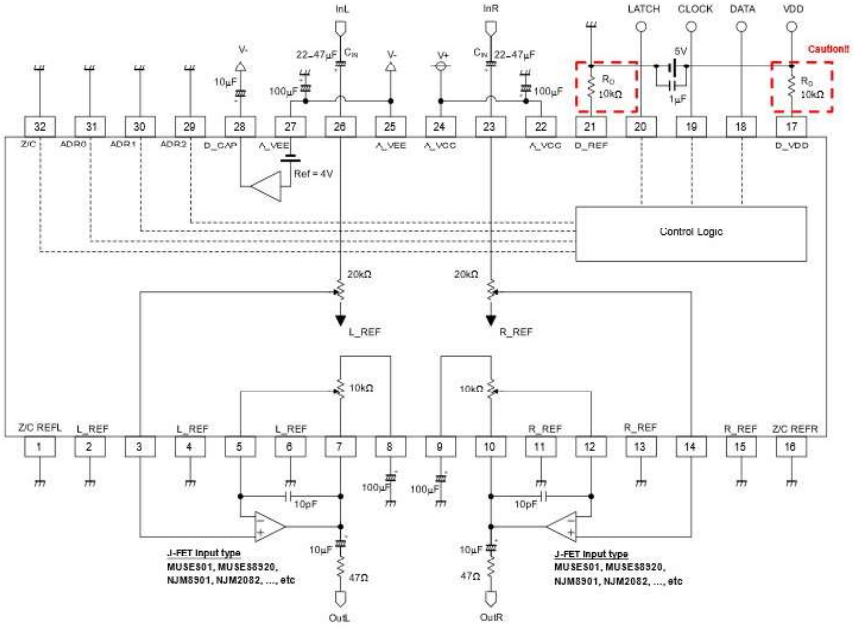
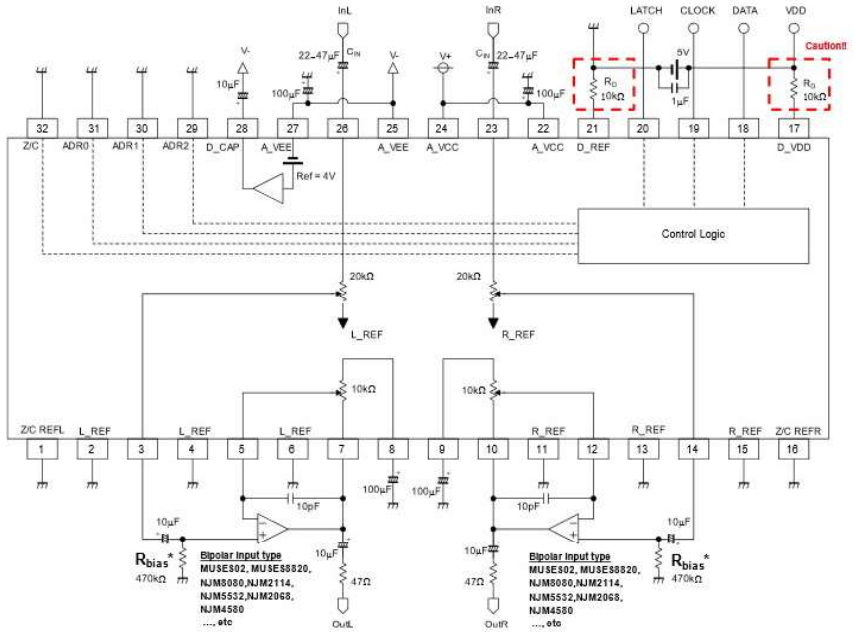
■ APPLICATION CIRCUIT

<Application circuit with **J-FET** Input type OpAmp.>

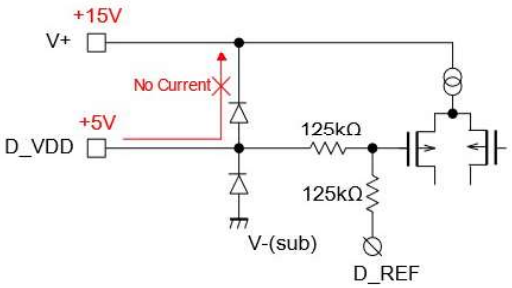


<Application circuit with **Bipolar** Input type OpAmp.>

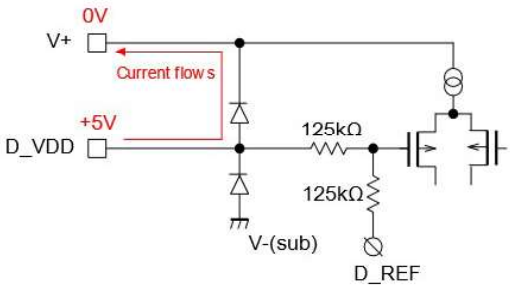


■ NOTES

It is necessary to add R_D to 10kΩ for the over-current protection. Without this resistor, the IC may be damaged, depending on the power procedure.



a) The power[V+] is greater than the power[D_VDD].



b) The power[V+] is less than the power[D_VDD].

Fig.1 Damaged path of the MUSES72320

The input coupling capacitors(C_{IN}) and the input resistance(R_{IN}=20kΩ) form a high-pass filter with the corner frequency determined in [$fc=1/(2\pi R_{IN}C_{IN})$].

The R_{bias} affects the Volume(Att.) linearity characteristic. When R_{bias} value is too small, the amount of attenuation increases, so that the output amplitude becomes small and THD deteriorates by an internal analog switch. On the other hand, when R_{bias} is too large, it may be affected at the noise from the outside. Please decide resistance value after it verifies it enough by an actual application.

Separate for REF terminals for High and Middle voltage(AC) and REF terminals for Low voltage(AC) in the pattern design.

Pin No.	Function	Purpose
2	Lch Reference Voltage	for Low voltage(AC) signal
4	Lch Reference Voltage	for Middle voltage(AC) signal
6	Lch Reference Voltage	for High voltage(AC) signal
11	Rch Reference Voltage	for High voltage(AC) signal
13	Rch Reference Voltage	for Middle voltage(AC) signal
15	Rch Reference Voltage	for Low voltage(AC) signal

Table.1 Purpose of Reference Voltage Terminal